



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/765,966	01/19/2001	Linkai Bu	87157656.242004	8230

23562 7590 10/05/2004

BAKER & MCKENZIE
PATENT DEPARTMENT
2001 ROSS AVENUE
SUITE 2300
DALLAS, TX 75201

EXAMINER

NGUYEN, LONG T

ART UNIT PAPER NUMBER

2816

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/765,966

Applicant(s)

BU ET AL.

Examiner

Long Nguyen

Art Unit

2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 January 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the “resistor” as recited in claim 5 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as “amended.” If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled “Replacement Sheet” in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 2 is objected to because of the following informalities:

Claim 2, line 4, “inverter generate” should be changed to --inverter to generate--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 1, the recitation “the power and ground levels of said system” on line 12 is indefinite because “the power” in the above phrase lacks antecedent basis, and it is unclear whether the power refers to the first lower voltage or the second higher voltage. It is suggested that “the power and ground levels of said system” on line 12 be changed to --a power supply terminal for providing a power having the second higher voltage level and a ground terminal of said system--. Further, it is also suggested to changed “the power end” on line 13 to -the power supply terminal--, and “the ground end” on line 14 to --the ground terminal--.

Also in claim 1, the recitation “said input logic family” on line 21 lacks clear antecedent basis, and it is not unclear whether it refers to the first logic family or the second logic family. Further, the recitation “the gate terminal of said first NMOS transistor serves as the signal input of said input logic family” on line 21-22 appears to be misdescriptive because it is unclear how the gate of the first NMOS can serves as the input of either one of the logic families since the level shifter is mainly used to interface between two circuits that have different voltage levels (i.e., the gate of the first NMOS transistor cannot be the input of either one of the input logic families). Clarification and/or appropriate correction is requested.

Also in claim 1, the recitation "to cut off said first and second PMOS transistors" on line 23-24 is indefinite because it is not clear how the first and second PMOS transistors being cut off, and/or cut off from what. It is suggested to changed "to cut off said first and second PMOS transistors" on line 23-24 to --to cut off the power to said first and second PMOS transistors--.

Claim 2 is indefinite because it includes the indefiniteness of claim 1.

Claim 2, "said output" on line 3 is indefinite because it is not clear which output that it refers to. It appears that "said output" should be changed to --said shifted output--. Further, the recitation "to generate a complementary pair of said shifted output" on the line 4-5 is indefinite because it is inconsistent with what has been claimed since it is recited earlier that the gate terminal of the first PMOS transistors serves as the level shifted output (see line 21 of claim 1), and it is now recited that the output of one of the two inverters (line 4-5 of claim 2) also generates the level shifted output, so it is not clear which one is actually the shifted output. Clarification and/or appropriate correction is requested.

With respect to claim 3, this claim (the recitations on lines 13-15, 21-22 and 26-27) is indefinite for the same reasons as discussed in claim 1 above.

Claims 4 and 5 are indefinite because it includes the indefiniteness of claim 3.

Also in claim 4, "a third PMOS transistor" on line 1 is misdescriptive since it is inconsistent with what is disclosed and shown in the drawings. Note that Figure 3 shows transistor 550 is an NMOS (not a PMOS) and it is recited on line 2 of claim 4 as "said NMOS transistor". Thus, it appears that "PMOS" on line 1 of claim 4 should be changed to --NMOS--.

With respect to claim 6, this claim (the recitations on lines 14-16, 22-23 and 29-30) is indefinite for the same reasons as discussed in claim 1 above.

Art Unit: 2816

Claim 7 is indefinite because it includes the indefiniteness of claim 6. Further, “the power level” on line 2 should also be changed to --the power supply terminal-- as suggested above.

With respect to claim 8, this claim (the recitations on lines 13-15, 21-22 and 24-25) is indefinite for the same reasons as discussed in claim 1 above.

Claim 9 is indefinite because it includes the indefiniteness of claim 8.

With respect to claim 10, this claim (the recitations on lines 12-14, 20-21 and 23-24) is indefinite for the similar reasons as discussed in claim 1 above. Further, the recitation “for shifting a signal of a first logic family at a first lower voltage level to a second higher voltage level of a second logic family” on lines 2-3 is misdescriptive since it is not consistent with the specification. Note that the specification discloses that Figure 7 is used to shift a first low-negative voltage signal into a high-negative voltage signal (e.g., shifting a first signal having the level swings between 0V and -3V to a second signal having a swing between 0V and -5V, and it is clear that $-5V < -3V$). Thus, the recitation “a first lower voltage level to a second higher voltage level” in the above phrase would be incorrect because, as shown in the example, the higher negative voltage is smaller than the less-negative voltage. Thus, it is suggest to change a “first lower voltage level to a second higher voltage level” on line 2-3 to --a first lower-negative voltage level to a second higher-negative voltage level--.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim 1 are rejected under 35 U.S.C. 102(e) as being anticipated by Tanaka et al. (USP 6,249,145).

With respect to claim 1, Figure 12 of the Tanaka et al. discloses a level-shifter circuit (516), which includes: a first PMOS (300), a first NMOS (304), a second PMOS (301), a second NMOS (305), a power-down control PMOS (314); the shifted output (the signal at the gate of 301), and the power control signal (the signal at the gate of 314 and 305). Note that the drain of first PMOS 300 is connected to the drain of the first NMOS 304 (by way of 302), and the drain of second PMOS 301 is connected to the drain of the second NMOS 305 (by way of 303).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 2-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (USP 6,249, 145) in view of Kim (USP 5,917,339).

With respect to claim 2, the level shifter (516) in Figure 12 of the Tanaka et al. reference meets all the limitations of this claim except that the level shifter including first and second inverters connected in series and connected to the output for providing a pair of complementary output signal. However, the Kim reference discloses in Figure 2 a level shifter circuit including first and second inverters (15-16) connected in series and connected to the output for the purpose of buffering the output signal for output driving (i.e., driving downstream circuitry). Therefore, it would have been obvious to one having skill in the art that the time the invention was made to modify the circuit in Figure 12 of the Tanaka et al. reference by providing series-connected first and second inverters to the output node (the node connected the drain of transistor 305 and the gate of transistor 300 together, Figure 12 of Tanaka et al.) for the purposes of buffering the output signal to improve the driving capability of the output signal. Thus, this modification meets all the limitations of claim 2. Note that the output of the first inverter, and the output of the second inverter in the above modification provide the pair of complementary of the output signal.

With respect to claim 3, the modification as discussed in claim 2 meets all the limitations of this claim, i.e., this claim is rejected for the same manner as in claim 2.

Insofar as understood in claim 4, Figure 12 of the Tanaka et al. reference in the above modification shows the level shifter circuit including a third NMOS transistor (313).

With respect to claim 5, Figure 12 of the Tanaka et al. reference in the above modification shows the level shifter circuit including a resistor (313, note that a MOSFET acts as a variable resistor due to the signal at the gate of the MOSFET controlling the resistance of the MOSFET).

With respect to claim 6, this claim is rejected for the same manner as in claim 4.

With respect to claim 7, the modification (Figure 12 of Tanaka et al. in view of Figure 2 of Kim) as discussed in claim 6 meets all the limitations of the claim except that the level shifter including a third PMOS transistor connected between the power supply terminal and the power-down control PMOS transistor. However, Figure 6 of the Tanaka et al. reference discloses a level shifter circuit including a PMOS transistor (306) connected between the power supply terminal (VDDQ) and the cross-coupled PMOS transistors of the level shifter for the purpose of ensuring the corrected operation of the circuitry under low power application (Col. 6, line 25-48 of Tanaka et al.). Therefore, it would have been obvious to modify the above modification (Figure 12 of Tanaka et al. in view of Figure 2 of Kim) by providing a third PMOS transistor directly connected to the power supply terminal (VDDQ) and between the power-down control PMOS transistor (313, Figure 12 of Tanaka et al.) for the purpose of ensuring the corrected operation of the level shifter under lower power application and thereby reducing power consumption. Thus, this modification meets all the limitations of claim 7.

With respect to claim 8, the modification discussed in claim 7 also meets the limitations of claim 8.

With respect to claim 9, the third PMOS transistor as discussed in claim 7 (i.e., transistor 306) is a constant source.

9. Claims 8-10 also are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (USP 6,249, 145).

With respect to claim 8, the level shifter circuit (516) in Figure 12 of the Tanaka et al. reference meets all the limitations of the claim (similar as discussed in claim 1 in the 102

Art Unit: 2816

rejection) except that the level shifter including a third PMOS transistor connected between the power supply terminal and the power-down control PMOS transistor. However, Figure 6 of the Tanaka et al. reference discloses a level shifter circuit including a PMOS transistor (306) connected between the power supply terminal (VDDQ) and the cross-coupled PMOS transistors of the level shifter for the purpose of ensuring the corrected operation of the circuitry under low power application (Col. 6, line 25-48 of Tanaka et al.). Therefore, it would have been obvious to modify the level shifter 516 in Figure 12 of the Tanaka et al. reference by providing a third PMOS transistor directly connected to the power supply terminal (VDDQ) and between the power-down control PMOS transistor (313, Figure 12 of Tanaka et al.) for the purpose of ensuring the corrected operation of the level shifter under lower power application and thereby reducing power consumption. Thus, this modification meets all the limitations of claim 8.

With respect to claim 9, the third PMOS transistor as discussed in claim 7 (i.e., transistor 306) is a constant source.

With respect to claim 10, Figure 12 of the Tanaka et al. reference discloses a level shifter circuit (516) which having the structure for shifting positive power supply voltages. The different between the prior art (Figure 12 of Tanaka et al.) and the claim invention is that the structure of the claim invention is for shifting the negative power voltages. However, it is notoriously well-known that a circuit operates with positive power supply voltage can be modify to operate with negative power supply voltage by replacing each NMOS transistor in the circuit with a PMOS transistor, and each PMOS transistor in the circuit with an NMOS transistor. Therefore, it would have been obvious to one having skill at the time the invention was made to modify the circuit in Figure 12 by replacing each NMOS transistor in the circuit with a PMOS

Art Unit: 2816

transistor, and each PMOS transistor in the circuit with an NMOS transistor for the purpose of operating the circuit with a particular power supply depending on the need of the designer (i.e., negative power supply in this case). Note that, in this modification, the power supply VDDQ is now a negative power supply. Thus, this modification meets all the limitations of claim 10 as it can be seen that the modification circuit (i.e., replacing each NMOS transistor in the circuit in Figure 12 with a PMOS transistor, and each PMOS transistor in the circuit with an NMOS transistor) including: a first PMOS (304), a first NMOS (300), a second PMOS (305), a second NMOS (301), a power-down control NMOS (314); the shifted output (the signal at the gate of 301), and the power control signal (the signal at the gates of 314 and 305). Note that the drain of first NMOS 300 is connected to the drain of the first PMOS 304 (by way of 302), and the drain of second NMOS 301 is connected to the drain of the second PMOS 305 (by way of 303).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

Art Unit: 2816

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

September 29, 2004

A handwritten signature in cursive script, appearing to read 'Long Nguyen', with a long horizontal flourish extending to the right.

Long Nguyen
Primary Examiner
Art Unit: 2816